REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1-50 are pending. Claims 1-50 have been rejected.

Claims 1, 2, 4, 5, 11, 12, 17, 25, 28, 29, 35, 36, and 41 have been amended. Claims 10 and 34 have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 102

Claims 11-24 and 35-48 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,397,324, to Barry, et al. ("Barry").

Amended claim 11 reads as follows

> A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
> receiving the single instruction;
> receiving a first vector having a plurality of numbers;
> partitioning look-up memory into a plurality of look-up tables;
> looking up simultaneously a plurality of elements of a second vector from the plurality of look-up tables, each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers;
> wherein the partitioning and the looking-up operations are performed in response to the microprocessor receiving the single instruction.

(Amended claim 11) (emphasis added).

The Examiner stated that "Barry has taught....receiving a first plurality of numbers (Barry, An/Ri of Fig. 4 or An/Rz of Fig. 8) and a second plurality of numbers (Barry Rs of Fig. 4 or Rte/Rto of Figure 8)..." (Office Action, p. 8, 11/02/05).

Applicants respectfully disagree.

Barry discloses an address register file (ARF), a compute register file (CRF), and two memory banks accessible by a dual address table look-up instruction (L2TBL) or store to table instruction (S2TBL). More specifically, Barry discloses that the L2TBL instruction contains two base addresses (An. H1 and An. H0) from the ARF, two offsets (Rze.H0 and Rzo.H0) from the CRF, and two target registers Rto and Rte from the CRF. The An.H0+Rze.H0 value addresses memory bank-0; and the An.H1+Rzo.H0 value addresses the memory bank-1. The data read from the memory bank-1 and memory bank-0 are loaded into target registers Rto and Rte specified in CRF (col. 10, lines 62-col.11, line 47).

Thus, Barry merely discloses a L2TBL instruction that specifies two base addresses and two offsets to read data from the memory banks, and to target addresses to load the data into CRF, in contrast to receiving a first vector having a plurality of numbers, as recited in amended claim 11. Additionally, Barry merely discloses that "the local data memories ...are currently organized as two memory banks to support independent, simultaneous accesses by the processing unit" (col. 7, lines 54-62), in contrast to partitioning look-up memory into a plurality of look-up tables in response to receiving the single instruction, as recited in amended claim 11. Further, Barry merely discloses looking up data from the memory banks (col. 8, line 62-col. 12, line 27), in contrast to looking up simultaneously a plurality of elements of a second vector from the plurality of look-up tables, each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers of the first vector.

Because Barry fails to disclose discussed limitations of amended claim 11, Applicants respectfully submit that amended claim 11 and claims 12-24 that depend from amended claim 11, are not anticipated by Barry under 35 U.S.C. § 102(e).

Given that amended claim 35 contains at least the discussed limitations of amended claim 11, Applicants respectfully submit that amended claim 35 and claims 36-50 that depend from amended claim 35 are not anticipated by Barry under 35 U.S.C. § 102(e).

Rejections Under 35 U.S.C. § 103

Claims 1-10, 25-26 and 49-50 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Barry, in view of U.S. Patent No. 5,768,628 to Priem ("Priem").

Amended claim 1 reads as follows.

> A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
>
> receiving the single instruction;
>
> receiving a first vector having a first plurality of numbers and a second vector having a second plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables; and
>
> replacing simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers;
>
> wherein the receiving and the replacing operations are performed in response to the microprocessor receiving the single instruction;
>
> wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit.

(Amended claim 1) (emphasis added)

Barry merely discloses a S2TBL instruction that uses address An.H0 + Rzo to store a byte, halfword, or word to a memory bank 0, and address An.H1+ Rze to store a byte, halfword, or word to the memory bank 1 (col. 11-lines 65-col. 12, line 27), and fails to disclose receiving a first vector having a first plurality of numbers and a second vector having a second plurality of numbers, each of the first plurality of numbers of the first vector pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables. Additionally, Barry merely discloses storing to two memory banks a byte, halfword, or word, in contrast to replacing simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers of the second vector, as recited in amended claim 1.

Priem discloses a system memory to store wave tables and a direct memory access controller to transfer the wave tables stored in the memory to a sound generator to generate a

voice. More specifically, Priem disclose that a command for a voice provides the address of the wave table and the parameters to be used to play the voice (col. 7 lines 29-34).

Thus, Priem, similarly to Barry, fails to disclose the limitations of amended claim 1 of receiving a first vector having a first plurality of numbers and a second vector having a second plurality of numbers, each of the first plurality of numbers of the first vector pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables. Additionally, Priem, similarly to Barry, fails to disclose replacing simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers of the second vector.

Consequently, even if Priem and Barry were combined, such a combination would lack the discussed limitations of amended claim 1.

Therefore, it is respectfully submitted that amended claim 1 and claims 2-3 that depend from amended claim 1 are not obvious under 35 U.S.C. § 103(a) in over Barry in view of Priem.

Given that claims 25-27 contain at least the discussed limitations of amended claim 1, it is respectfully submitted that claims 25-27 are not obvious under 35 U.S.C. § 103(a) in over Barry in view of Priem.

Applicants have amended claim 5 to include receiving the single instruction having an identity number code that specifies a DMA controller. Replacing at least one entry for each of a plurality of look-up units in a microprocessor with a plurality of numbers using the Direct Memory Access (DMA) controller is performed in response to the microprocessor receiving the single instruction.

Barry merely discloses a store to table instruction that uses addresses An.H + Rz to store a byte, halfword, or word to memory banks (col. 11-lines 65-col. 12, line 27).

Priem merely discloses that a command for a voice provides the address of the wave table and the parameters to be used to play the voice (col. 7 lines 29-34).

Thus, neither Barry, nor Priem discloses the limitation of amended claim 6 of receiving the single instruction having an identity number code that specifies a DMA controller; and replacing at least one entry for each of a plurality of look-up units in a microprocessor with a plurality of numbers using the Direct Memory Access (DMA) controller is performed in response to the microprocessor receiving the single instruction, as recited in amended claim 5.

Furthermore, even if Barry and Priem were combined, such a combination would lack receiving the single instruction having an identity number code that specifies a DMA controller, as recited in amended claim 5.

Therefore, it is respectfully submitted that amended claim 5 not obvious under 35 U.S.C. § 103(a) in over Barry in view of Priem.

Because amended claims 4, 28, and 29 contain at least the discussed limitations, Applicants respectfully submit that amended claims 4, 28, and 29 are not obvious under 35 U.S.C. § 103(a) over Barry in view of Priem.

Because claims 6-9, 30-33, and 49 depend from respective amended claims 5 and 29, and add additional limitations, Applicants respectfully submit that claims 6-9, 30-33, and 49 are not obvious under 35 U.S.C. § 103(a) over Barry in view of Priem.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections of all pending claims have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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Date: 2/28/2006

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